What is claimed is:

1. A field programmable gate array architecture comprising:

a plurality of horizontal routing channels each including a plurality of interconnect conductors, some of said interconnect conductors segmented by user-programmable interconnect elements;

a plurality of vertical routing channels each including a plurality of interconnect conductors forming intersections with interconnect conductors in said horizontal routing channels, some of said interconnect conductors segmented by user-programmable interconnect elements;

user-programmable interconnect elements connected between selected ones of said horizontal and vertical interconnect conductors at selected ones of said intersections;

an array comprising a plurality of rows and columns of logic function modules superimposed on said horizontal and vertical routing channels, each of said logic function modules having at least one input and at least one output, said at least one input and at least one output of said logic function modules connectable to ones of said interconnect conductors in either or both of said horizontal and vertical routing channels;

at least a portion of one column of said array including random access memory blocks disposed in said array in place of logic function modules, said at least a portion of a column adjacent to at least one column of said logic function modules, each of said random access memory blocks spanning a distance of more than one row

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of said array such that at least one interconnect conductor in more than one horizontal routing channel passes therethrough and is connectable to adjacent logic function modules on either side thereof; each of said random access memory blocks having address inputs, control inputs, data inputs, and data outputs;

user-programmable interconnect elements connected between said address inputs, control inputs, data inputs, and data outputs of said random access memory blocks and selected ones of said interconnect conductors in said more than one horizontal routing channel passing therethrough; and

means for programming selected ones of said user-programmable interconnect conductors to connect the at least one input and at least one output of ones of said logic function modules to one another and to the address inputs, control inputs, data inputs, and data outputs of said random access memory blocks.

2. The field programmable gate array architecture of claim 1 wherein said random access memory blocks are dual ported static random access memory blocks.

3. The field programmable gate array architecture of claim 1 wherein one of said control inputs of said random access memory blocks is a mode control input for selecting between a first data bus width and a second data bus width.

4. The field programmable gate array architecture of claim 3 wherein said first data bus width is eight bits and said second data bus width is four bits.

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5. The field programmable gate array architecture of claim 1 wherein one of said control inputs of said random access memory blocks is a write clock input polarity control input having two states, a first state in which write operations are initiated on a rising edge of a write clock input to said random access memory blocks and a second state in which write operations are initiated on a falling edge of said write clock input.

6. The field programmable gate array architecture of claim 1 wherein said random access memory blocks include a block enable input for enabling said random access memory blocks and wherein one of said control inputs of said random access memory blocks is a block enable input polarity control input having two states, a first state in which said random access memory blocks are enabled by a logic high signal on said block enable input to said random access memory blocks and a second state in which said random access memory blocks are enabled by a logic low signal on said block enable input.

7. The field programmable gate array architecture of claim 1 wherein said random access memory blocks include read address latches and read data output latches, each of said read address latches and read data output latches having a transparent state and a latched state, the transparent states and the ~~read~~ latched states of the read address latches and read data output latches being responsive to opposite logic

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states of a read clock input to said random access memory blocks.

8. A field programmable gate array architecture comprising:

a plurality of horizontal routing channels each including a plurality of interconnect conductors, some of said interconnect conductors segmented by user-programmable interconnect elements;

a plurality of vertical routing channels each including a plurality of interconnect conductors forming intersections with interconnect conductors in said horizontal routing channels, some of said interconnect conductors segmented by user-programmable interconnect elements;

user-programmable interconnect elements connected between selected ones of said horizontal and vertical interconnect conductors at selected ones of said intersections;

an array comprising a plurality of rows and columns of logic function modules superimposed on said horizontal and vertical routing channels, each of said logic function modules having at least one input and at least one output, said at least one input and at least one output of said logic function modules connectable to ones of said interconnect conductors in either or both of said horizontal and vertical routing channels;

at least a portion of more than one column of said array including random access memory blocks disposed in said array in place of logic function modules, said at least a portion of more than one column adjacent to at least one column of said logic

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function modules, each of said random access memory blocks spanning a distance of more than one row of said array such that at least one interconnect conductor in more than one horizontal routing channel passes therethrough and is connectable to adjacent logic function modules on either side thereof; each of said random access memory blocks having address inputs, control inputs, data inputs, and data outputs;

user-programmable interconnect elements connected between said address inputs, control inputs, data inputs, and data outputs of said random access memory blocks and selected ones of said interconnect conductors in said more than one horizontal routing channel passing therethrough; and

means for programming selected ones of said user-programmable interconnect conductors to connect the at least one input and at least one output of ones of said logic function modules to one another and to the address inputs, control inputs, data inputs, and data outputs of said random access memory blocks.

9. The field programmable gate array architecture of claim 8 wherein said random access memory blocks are dual ported static random access memory blocks.

10. The field programmable gate array architecture of claim 8 wherein one of said control inputs of said random access memory blocks is a mode control input for selecting between a first data bus width and a second data bus width.

11. The field programmable gate array architecture of claim 10 wherein said

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first data bus width is eight bits and said second data bus width is four bits.

12. The field programmable gate array architecture of claim 8 wherein one of said control inputs of said random access memory blocks is a write clock input polarity control input having two states, a first state in which write operations are initiated on a rising edge of a write clock input to said random access memory blocks and a second state in which write operations are initiated on a falling edge of said write clock input.

13. The field programmable gate array architecture of claim 8 wherein said random access memory blocks include a block enable input for enabling said random access memory blocks and wherein one of said control inputs of said random access memory blocks is a block enable input polarity control input having two states, a first state in which said random access memory blocks are enabled by a logic high signal on said block enable input to said random access memory blocks and a second state in which said random access memory blocks are enabled by a logic low signal on said block enable input.

14. The field programmable gate array architecture of claim 8 wherein said random access memory blocks include read address latches and read data output latches, each of said read address latches and read data output latches having a transparent state and a latched state, the transparent states and the ~~read~~ latched states of the

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read address latches and read data output latches being responsive to opposite logic states of a read clock input to said random access memory blocks.

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